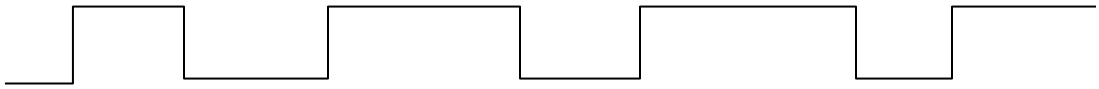
*) State whether the following statements correct or not, if not state the correct answer.

1) Signals that connect the system with its environment are specified as ports.(T)
2) Bus width is implicitly defined by the bit order in the definition.(T)
3) If a signal is declared in a package, which is used by an entity, then the use clause must be applied in architecture of this entity as well.(F)
4) Left bound of the order of bits in a vector must always be smaller than the right bound.(F)
5) Each port must be specified with mode.(T)
6) A port mode specifies the information about the direction of data flow through the port.(T)
7) Ports are signals.(T)
8) Set of states of a finite state machine is usually declared as enumeration type.(T)
9) Logical operators can be applied to single bits only.(F)
10) Each process must be assigned a name.(F)

*) Write the VHDL code of a circuit to generate a waveform with the following characteristics and with an enable signal:



10 ns 20 ns 30 ns 40 ns 50 ns 60 ns

answer:

```
library ieee;

use ieee.std_logic_1164.all;

entity clock is

port ( en : in std_logic;

        clk: inout std_logic :='0') ;

end clock ;

architecture behave of clock is

begin
```

```
process (en, clk)

begin

clk <= not clk after 10 ns;

End process;

End behave;
```

*) Determine the type of the following VHDL code and its function:

ror, *natural, Signal _name'* **last_event** , **scalar_type'**ascending, *others* , **to_bit(expression)**.

Answer:

	Type	function
Signal _name' last_event	attribute	returns the time interval since the last event on the signal
scalar_type' ascending	attribute	True if T is an ascending range, otherwise False
ror	Shift operator	Rotate right
others	statement	used to indicate all unspecified elements and if used, it must be last item in the list.
to_bit	function	To convert std_logic to bit
Natural	Predefined data type	Integer starting with 0 up to the max specified in the implementation

*) Write a VHDL code for a sequence detector that detects the pattern 1110.